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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,789	01/30/2002	Masatoshi Kokubun	100353-00095	4716

7590 03/09/2005

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EXAMINER

JELINEK, BRIAN J

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/058,789

Applicant(s)

KOKUBUN ET AL.

Examiner

Brian Jelinek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 5-10, 15-24, and 31-36 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 11-14, 25 and 26 is/are rejected.
- 7) ☒ Claim(s) 27-30 is/are objected to.
- 8) ☒ Claim(s) 1-36 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1/30/2002.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

This is a first office action in response to application no. 10/058,789 filed on 1/30/2002 in which claims 1-36 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

During a telephone conversation with Rustan Hill (Reg. #37351) on 1/28/2005 a provisional election was made without traverse to prosecute the invention of Species III, claims 1-4, 11-14, and 25-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 5-10, 15-24, and 31-36 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

This application contains claims directed to the following patentably distinct species of the claimed invention:

Species I: Fig. 7

Species II: Fig. 8

Species III: Figs. 9 and 10

Species IV: Fig. 11

Species V: Fig. 12

Species VI: Fig. 17

Species VII: Fig. 18

If the applicant elects species V, it is further required they elect a single disclosed group of sub-species for prosecution on the merits from the following sub-species.

Sub-species A: Fig. 13

Sub-species B: Fig. 14

Sub-species C: Fig. 15

Sub-species D: Fig. 16

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 1 and 2 are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims

are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Masuyama (U.S. Pat. No. 6,674,471).

Regarding claim 1, Masuyama discloses a CMOS sensor circuit (Figs. 1 and 10a) comprising: a photodiode (Fig. 2, element 3); a reset transistor resetting said photodiode to an initial voltage (Fig. 2, element 7); and a voltage control circuit (Fig. 10A) controlling a gate potential of said reset transistor to a potential other than power source potentials (Fig. 10B, Vss1).

Regarding claim 2, Masuyama discloses a CMOS sensor circuit (Figs. 1 and 10a) comprising: a photodiode (Fig. 2, element 3); a reset transistor resetting said photodiode to an initial voltage (Fig. 2, element 7); and a voltage control circuit (Fig. 10A) keeping a gate potential of said reset transistor from completely becoming off (Fig. 10B, Vss1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-4, 11-14, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuyama (U.S. Pat. No. 6,674,471), in view of Maki (U.S. Pat. No. 5,907,357), and further in view of Fuji (U.S. Pat. No. 5,768,203).

Regarding claim 3, Masuyama discloses a voltage control circuit to suppress blooming comprises: an inverter circuit driving a gate of the reset transistor, the inverter

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circuit including a first P-channel MOS transistor and an N-channel MOS transistor (Fig. 10A). Masuayama does not disclose a transistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor.

However, Maki discloses a voltage control circuit (Fig. 5) comprises: an inverter circuit driving a gate of a reset transistor (Fig. 5, element 11 and 12), the inverter circuit including a first P-channel MOS transistor (Fig. 5, element Q13) and an N-channel MOS transistor (Fig. 5, element Q14); and a resistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor (Fig. 5, element R). One of ordinary skill in the art would have provided the voltage control circuit of Maki for the purpose of prolonging the fall time of the reset pulse (col. 6, lines 21-26). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the voltage control circuit of Maki for the purpose of prolonging the fall time of the reset pulse.

Maki does not disclose the resistor may be configured as a transistor. However, Fuji discloses a P-MOS transistor acts as a resistor when its gate and drain are connected (col. 5, lines 64-66). One of ordinary skill in the art would have configured a resistor as a P-MOS transistor with its gate and drain connected because it is well known in the art that a P-MOS transistor thus connected acts as a resistor (col. 5, lines 64-66). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel a MOS transistor because it is well known in the art that a P-MOS transistor with its gate and drain connected acts as a resistor.

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Regarding claim 4, please see the 103 rejection of claim 3.

Regarding claim 11, please see the 103 rejection of claim 3.

Regarding claim 12, please see the 103 rejection of claim 3.

Regarding claim 13, please see the 103 rejection of claim 3.

Regarding claim 14, please see the 103 rejection of claim 3.

Regarding claim 25, Masuyama discloses a voltage control circuit to suppress blooming, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, and an N-channel MOS transistor having a gate supplied with a second signal. Masuyama does not teach an additional transistor.

However, Maki discloses a voltage control circuit (Fig. 5) comprises an inverter circuit driving a gate of said reset transistor (Fig. 5, element 11 and 12), the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal (Fig. 5, element Q13), an N-channel MOS transistor having a gate supplied with a second signal (Fig. 5, element Q14); and a resistor (Fig. 5, element R). One of ordinary skill in the art would have provided the voltage control circuit of Maki for the purpose of prolonging the fall time of the reset pulse (col. 6, lines 21-26). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the voltage control circuit of Maki for the purpose of prolonging the fall time of the reset pulse.

Maki does not disclose the resistor may be configured as a transistor. However, Fuji discloses a P-MOS transistor acts as a resistor when its gate and drain are

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connected (col. 5, lines 64-66). One of ordinary skill in the art would have configured a resistor as a P-MOS transistor with its gate and drain connected because it is well known in the art that a P-MOS transistor thus connected acts as a resistor (col. 5, lines 64-66). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel a MOS transistor because it is well known in the art that a P-MOS transistor with its gate and drain connected acts as a resistor.

Regarding claim 26, please see the 103 rejection of claim 25.

Allowable Subject Matter

Claims 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 27-28, the reason for allowance is as follows: the prior art does not disclose or fairly suggest a delay circuit.

Regarding claims 29-30, the reason for allowance is as follows: the claims depend from allowable base claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (703) 305-

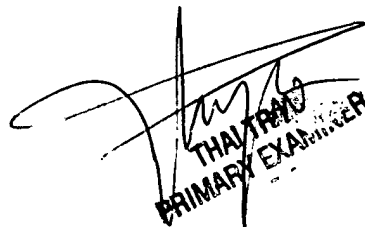
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4724 until 3/2/2005, and (571)272-7366 thereafter. The examiner can normally be reached on M-F 8:00 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Thai Tran can be reached at (703) 305-4725. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
3/7/2005



THAI TRAN
PRIMARY EXAMINER